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EXAMINER

NATNAEL, PAULO S M

ART UNIT	PAPER NUMBER
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2614

DATE MAILED: 05/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/922,141

Applicant(s)

KUEHN, HANS JUERGEN

Examiner

Paulos M. Natnael

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 August 2001 (preliminary amendment).
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 and 14 is/are rejected.
- 7) ☒ Claim(s) 13 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 August 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 6 and 7.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. The fee calculation shows one independent claim (claim 1), however, claim **14** is also an independent claim. Appropriate fee correction is required.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, in claim **13**, the claimed "...eight npn transistors (14) and 24 pnp transistors (16) are provided, and in that the four-stage adapter circuit (10) or the four adapter stages (10) precede a resistor (50)" and in claim **12**, "that the adapter circuit (10) is multi-staged and/or more than one adapter circuit (10) is provided" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The abstract of the disclosure is objected to because the abstract is not in one paragraph. Correction is required. See MPEP § 608.01(b).

Content of Specification

- (a) Title of the Invention: See 37 CFR 1.72(a) and MPEP § 606. The title of the invention should be placed at the top of the first page of the specification unless the title is provided in an application data sheet. The title of the invention should be brief but technically accurate and descriptive, preferably from two to seven words may not contain more than 500 characters.
- (b) Cross-References to Related Applications: See 37 CFR 1.78 and MPEP § 201.11.
- (c) Statement Regarding Federally Sponsored Research and Development: See MPEP § 310.
- (d) Incorporation-By-Reference Of Material Submitted On a Compact Disc: The specification is required to include an incorporation-by-reference of electronic documents that are to become part of the permanent United States Patent and Trademark Office records in the file of a patent application. See 37 CFR 1.52(e) and MPEP § 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text were permitted as electronic documents on compact discs beginning on September 8, 2000.

Or alternatively, Reference to a "Microfiche Appendix": See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.
- (e) Background of the Invention: See MPEP § 608.01(c). The specification should set forth the Background of the Invention in two parts:
 - (1) Field of the Invention: A statement of the field of art to which the invention pertains. This statement may include a paraphrasing of the applicable U.S. patent classification definitions of the subject matter of the claimed invention. This item may also be titled "Technical Field."
 - (2) Description of the Related Art including information disclosed under 37 CFR 1.97 and 37 CFR 1.98: A description of the related art known to the applicant and including, if applicable, references to specific related art and problems involved in the prior art which are

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solved by the applicant's invention. This item may also be titled "Background Art."

- (f) Brief Summary of the Invention: See MPEP § 608.01(d). A brief summary or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract and is directed toward the invention rather than the disclosure as a whole. The summary may point out the advantages of the invention or how it solves problems previously existent in the prior art (and preferably indicated in the Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the nature and gist of the invention or the inventive concept should be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention.
- (g) Brief Description of the Several Views of the Drawing(s): See MPEP § 608.01(f). A reference to and brief description of the drawing(s) as set forth in 37 CFR 1.74.
- (h) Detailed Description of the Invention: See MPEP § 608.01(g). A description of the preferred embodiment(s) of the invention as required in 37 CFR 1.71. The description should be as short and specific as is necessary to describe the invention adequately and accurately. Where elements or groups of elements, compounds, and processes, which are conventional and generally widely known in the field of the invention described and their exact nature or type is not necessary for an understanding and use of the invention by a person skilled in the art, they should not be described in detail. However, where particularly complicated subject matter is involved or where the elements, compounds, or processes may not be commonly or widely known in the field, the specification should refer to another patent or readily available publication which adequately describes the subject matter.
- (i) Claim or Claims: See 37 CFR 1.75 and MPEP § 608.01(m). The claim or claims must commence on separate sheet or electronic page (37 CFR 1.52(b)(3)). Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. There may be plural indentations to further segregate subcombinations or related steps. See 37 CFR 1.75 and MPEP § 608.01(i)-(p).
- (j) Abstract of the Disclosure: See MPEP § 608.01(f). A brief narrative of the disclosure as a whole in a single paragraph of 150 words or less commencing on a separate sheet following the claims. In an international application which has entered the national stage (37 CFR 1.491(b)), the applicant need not submit an abstract commencing on a separate sheet if

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an abstract was published with the international application under PCT Article 21. The abstract that appears on the cover page of the pamphlet published by the International Bureau (IB) of the World Intellectual Property Organization (WIPO) is the abstract that will be used by the USPTO. See MPEP § 1893.03(e).

- (k) Sequence Listing. See 37 CFR 1.821-1.825 and MPEP §§ 2421-2431. The requirement for a sequence listing applies to all sequences disclosed in a given application, whether the sequences are claimed or not. See MPEP § 2421.02.

Claim Objections

4. Claim **11** objected to because of the following informalities: the definition “Syndicat des Constructeurs d'Appareils Radii Receteurs et Televiscurs” is not in the English language. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims **1, 3-6, 8, 12 and 14** are rejected under 35 U.S.C. 102(b) as being anticipated by Scheraga, U.S. Pat. No. 5,789,955.

Considering claim **1**, Scheraga discloses all claimed subject matter, note;

a) a circuit arrangement, particularly for a Television, multimedia, radio or video recording device, for transition from a range of low voltage (U_i) to a range of high voltage (U_o), characterized in that at least one adapter circuit (10) is provided, which amplifies a particularly analog input signal of a low current (I_i) by an amplification factor (n) into a particularly analog output signal of a higher current (I_o), is met by the circuit arrangement utilized in radio or television illustrated in Fig.3 which has an input voltage of 5V V_{cc} and the output voltage is connected/assigned to the VBAT 12V and whose input current is approximately 0.2mA and has an output current that "...is multiplied by a factor referred to as beta, and appears at the collector current I_c that is caused to flow through the output load resistor, REXT". (see col. 5, lines 40-44)

b) the claimed "whose input (12) is assignable to the range of low voltage (U_i)," is met by the 5 V_{cc} , Fig.3, which is connected to the input stage.

c) the claimed, "whose output (18) is assignable to the range of higher voltage (U_o)", is met by the high voltage source 12V, fig. 3, that is connected to the output stage.

d) the claimed, comprises at least one npn transistor current mirror (14), is met by npn transistor current mirror circuit, fig.3.

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e) the claimed, at least one pnp current mirror (16) arranged in series with the npn transistor current mirror (14) and connected to at least one high voltage source (30), is met by the pnp current mirror circuit (fig. 3), which is connected to voltage source VBAT 12V, fig.3 and that "an NPN transistor current mirror and a PNP current mirror [are] connected in series". (see Abstract)

Considering claim 3, a circuit arrangement as claimed in claim 1, characterized in that the signal is amplified in the pnp current mirror (16) or in the npn transistor current mirror (14), is met by the PNP current mirror circuit (fig.3). (see also col. 5, lines 15-20)

Considering claim 4, a circuit arrangement as claimed in claim 1, characterized in that the high voltage source (30) supplies a voltage of the order of approximately 12 V, is met by the VBAT 12V output voltage source, Fig.3.

Considering claim 5, a circuit arrangement as claimed in any one of claim 1, characterized in that the input (12) ...is preceded by at least one supply or driver circuit (40) by which the low current (I) input signal can be applied to the adapter circuit (10), is met by voltage supply VCC (5.0V) and R3, fig.3;

Considering claim 6, a circuit arrangement, as claimed in claim 5, characterized in that the supply or driver circuit (40) is connected to at least one low voltage source (42).

Regarding claim 6, see rejection of claim 5.

Considering claim 8, Scheraga discloses the following claimed subject matter, note;

a) the npn transistor arrangement (14) is constituted as an npn current mirror and/or particularly as an NMOS current mirror (NMOS = N-channel Metal Oxide Semiconductor = N-channel Metal Oxide Semiconductor), is met by the NPN current mirror circuit, fig.3;

b) the pnp transistor arrangement (16) is constituted as a pnp current mirror and/or particularly as a PMOS current mirror (PMOS = P-channel Metal Oxide Semiconductor = P-type Metal Oxide Semiconductor), is met by the PNP current mirror circuit, fig.3.

Considering claim 12, a circuit arrangement wherein the circuit is multi-staged is met by input stage, the pnp current mirror stage, and the npn current mirror stage, and the output stage (fig.3). (Note: Since the claim is recited in the alternative, the examiner is meeting the first part in the and/or alternative).

Considering claim 14, a television, multimedia, radio or video recording device comprising at least a circuit arrangement (100) as claimed in claim 1.

Regarding claim 14, see rejection of claim 1.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims **2,7,9-11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Scheraga, U.S. Pat. No. **5,789,955**.

Considering claim **2**, a circuit arrangement as claimed in claim 1, characterized in that the amplification factor (n) is approximately 5.

Regarding claim 2, Scheraga discloses that the output current "...is multiplied by a factor referred to as beta, and appears at the collector current I_c that is caused to flow through the output load resistor, R_{EXT} ". (see col. 5, lines 40-44) Scheraga however does not specifically give a number or a factor for amplification. Nevertheless, it would have been an obvious matter of design choice to modify the system of Scheraga (which does not disclose a specific amplification factor or number but nonetheless utilizes some amplification factor or number to amplify the signal) by providing an amplification factor of 5 or such other similar number, given the resulting expectation of similar desired output or effect of minimizing and reducing electromagnetic interference or noise of the signal at the output of both the Scheraga reference and the claimed invention.

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Considering claim 7, a circuit arrangement as claimed in claim 6, characterized in that the low voltage source (42) supplies a voltage of the order of approximately 1 V to approximately 3.3V;

Regarding claim 7, Scheraga discloses 5 Vcc supply as the low voltage source for the input of the device. However, it would have been an obvious matter of design choice to modify the system of Scheraga by providing a lower voltage source between approximately 1 V to 3.3 V, since applicant has not disclosed that having such range of low voltage solves any stated problem or is for any particular purpose and it appears that a similar voltage would perform equally well.

Considering claim 9, a circuit arrangement characterized in that the output (18) of the adapter circuit (10) precedes at least a resistor (50) for converting the higher current (I_o) output signal into a higher voltage (U_o) output signal;

Regarding claim 9, Scheraga discloses an external Resistor (R_{ext}). However, doesn't disclose a resistor at the output 18 in order convert the current into voltage. Nevertheless, the examiner takes Official Notice in that it is notoriously well known in the electronic art to utilize resistor(s) connected from the output to ground to convert the output current into output voltage and, therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Scheraga by providing a resistor in order to be able to determine the output voltage of the circuit so that it would be used to drive the next stage.

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Considering claim **10**, the claimed a circuit arrangement as claimed in claim 9, characterized in that the resistor (50) has a value of approximately 1 K ohms.

Regarding claim 10, Scheraga does not discloses a resistor at the output 18; However, as shown above in claim 9, it is notoriously well known to employ a resistor to convert current to output voltage by utilizing a resistor, and therefore, it would be an obvious matter of design choice to select a value of the resistance according to the desired output value or level and modify the system of Scheraga accordingly.

Considering claim **11**, a circuit arrangement as claimed in claim 1, characterized in that the output (18) of the adapter circuit (10) precedes at least a SCART (= Syndicat des Constructeurs d'Appareils Radii Receteurs et Televiscurs) output (70).

Regarding claim 11, Scheraga does not specifically disclose a SCART socket. However, the Examiner takes Official Notice here in that the SCART socket is well known in the art for use in input and/or output terminals of circuits such as amplifiers and, thus, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Scheraga by providing a SCART socket at the output of the amplifier so that the system would be able to determine or check what sort of signal is being transmitted from current mirror stage to the next stage and thus have control of the transmitted signals.

Allowable Subject Matter

9. Claim **13** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: the prior art, Scheraga, fails to disclose a circuit arrangement wherein eight npn transistors and 24 pnp transistors are provided and in that a four-stage adapter circuit or four adapter stages precede a resistor, as in claim **13**;

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.


Kato et al, U.S. Pat. No. **5,724,519** discloses a complementary transistor circuit and amplifier and CRT display device using the same.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paulos Natnael
May 3, 2004


PAULOS M. NATNAEL
PATENT EXAMINER